DSN Programmed Oscillator

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This article describes the programmed oscillator installed in the DSN Block III receiver/exciter subsystem at DSS 14 and DSS 43 for Pioneer 10 support during the Jupiter flyby. A brief description is given of the Block III receiver/exciter subsystem modifications required to implement the programmed oscillator and design changes to add the capability of providing timed linear frequency sweeps in the manual operating mode.

I. Introduction

Programmed oscillator development for the Block III receiver/exciter has been described in a previous progress report (Ref. 1). Additional capability was incorporated to provide operator-selected timed frequency ramps for high-rate doppler tracking. Programmed oscillators were installed in the Block III receiver/exciter subsystems at DSS 14 and DSS 43 to support Pioneer 10 tracking during the Jupiter flyby.

II. Block III Receiver/Exciter Modification

Modifications to the Block III exciter and receiver to incorporate the programmed oscillator are described in the following.

A. Exciter

The programmed oscillator is inserted into the exciter (Fig. 1) at 66 MHz by mixing the Dana Synthesizer output frequency with the 5-MHz standard frequency multiplied by 4 in a new RF module exciter–mixer. The exciter–mixer replaces the $\times 3$ frequency multiplier and distribution module providing doppler extractor references, an exciter frequency monitor at 22 MHz, and 22 MHz to the tracking data handling subsystem (TDH). Exciter channel frequencies are selected and exciter tuning is accomplished using the exciter programmed oscillator control panel. The output frequency of the programmed oscillator, f_{SYNTH}, is determined as follows:

$$f_{SYNTH} = \frac{f_{XMT}}{32} - 4f_{REF}$$

f_{XMT} = S-band channel frequency (MHz)

f_{REF} = 5-MHz station standard

The exciter frequency $f_{XMT}/96$ (22 MHz) is monitored on the frequency counter as previously provided. Exciter tuning using the programmed oscillator control panel replaces the previously used exciter loop controls.

B. Receiver

The programmed oscillator is inserted into the receiver loop at 70 MHz (Fig. 2) as previously described in Ref. 2. The VCO is operated at 7 MHz with a gain of 400 Hz/V to retain the existing loop gain. The synthesizer output frequency is summed with a voltage-controlled oscillator (VCO) in a new RF module (RCVR VCO & MIXER). The output frequency (70 MHz) is divided by 3 to retain the receiver frequency monitor at 22 MHz.

Receiver tuning is accomplished with the programmed oscillator control panel replacing the previously used VCO and ACQUISITION controls.

The received frequency (f_{RCV}) is related to the programmed oscillator output frequency (f_{SYNTH}) as follows:

$$f_{RCV} = 32\,(f_{SYNTH} + f_{VCO}) + 50\,\text{MHz}$$

$$f_{VCO} = 3\,(7.0000\,\text{MHz}) \pm 3\Delta f$$

Δf is the residual offset of the VCO. Selection of the programmed oscillator output frequency (f_{SYNTH}) for receiver acquisition is as follows:

$$f_{SYNTH} = \frac{f_{RCV} - 50\,\text{MHz}}{32} - f_{VCO}$$

The receiver frequency monitor $f_{RCV\,VCO}$ is retained for compatibility with existing predict format by providing a divide-by-3 stage at the output of the receiver VCO and mixer; thus

$$f_{RCV\,VCO} = \frac{f_{RCV} - 50}{96} = \frac{f_{SYNTH} + f_{VCO}}{3}$$

Figure 3 is typical of the RF subassemblies installed to adapt the Block IV programmed oscillators to the Block III receiver and exciter. Figure 4 is a photograph of the cabinet assembly containing the programmed oscillators and the frequency and timing subsystem (FTS) interface used to translate and distribute station binary coded decimal (BCD) time codes to the programmed oscillators.

III. Programmed Oscillator Modifications

Both the control assembly and the synthesizer have been modified to increase capability. The programmed oscillator control described in Ref. 1 was modified to provide manually programmable timed linear frequency ramps. Front panel controls and storage registers were added to enable the subsystem operator to manually store in advance a timed sequence of four tuning rates without further adjustment during this tracking period. In addition, the four rate values can be refreshed to provide several additional timed frequency ramps during a tracking period. Ramp rates selectable from 10 μHz/s to 10 kHz/s (see Ref. 1) with start times (h:m:s) in increments of 1 s can be used.

The digiphase synthesizer described in Ref. 1 was modified to improve the phase control resolution and reduce radiated RF leakage. These modifications are described in the following:

A. Control Modifications

The added manual controls and displays provide the capability to visually monitor the programmed oscillator operation, to inspect stored control register contents and to manually operate the programmed oscillator. The added controls provide flexibility in the manual selection of frequency ramp rates and related monitoring. One section of pushbutton controls (see the front panel, Fig. 5), provides addressing and selection of one of the four rate registers that will control the frequency register when a sweep is initiated. The addressing permits storage of BCD selector switch contents and inspection of stored contents. Pushbuttons located at the center of the front panel control the sweep activation and termination. These pushbutton controls are described below.

(1) The SWP pushbutton initiates or terminates the frequency ramp at the current selected rate as indicated by the SWP light ON or OFF. (2) The TRK pushbutton turns the TRK light ON or OFF and if ON arms the control logic to automatically turn the SWP light ON when the stored time of the selected rate equals station time plus 1 s. Thereafter, the TRK light ON enables the succeeding rates to be selected at the next rate start time equals station time plus 1 s. (3) The LIM ENBL pushbutton turns the LIM ENBL light ON or OFF and if ON arms the control logic to terminate the frequency ramp and the TRK mode when the frequency reaches the stored upper or lower limit towards which the frequency is advancing. (4) The ACQ pushbutton arms the control logic when the ACQ light is ON to produce a triangular frequency sweep between the stored upper and lower limits when the SWP light is ON, and terminates the sweep when an external acquisition signal (ATZ) is received from an acquisition detector.

The choice of four rate and time registers was a compromise based on reasonable and adequate manual programming capability, limited panel space for manual controls and the existence of a transistor–transistor logic (TTL) medium scale integrated (MSI) circuit "4 × 4 register file" suited to this application. This integrated circuit (IC) contains 16 bits of read/write storage addressable as 4 words of 4 bits each. This IC features "read while write," and is implemented in the control to permit storage of a new rate and time digital code while simultaneously controlling the frequency at one of the other three previously stored codes. In addition, it permits continuous monitoring of any of the stored codes while concurrently controlling at a selected code. This is accomplished by applying a digital address code that alternately enables the contents of the selected control rate to be transferred to a control latch and the contents of the desired rate for display to be transferred to a display latch. The register addressing code is produced by depressing the corresponding rate pushbutton. Storage of a new rate value into one of the 4 addresses occurs by depressing the appropriate rate pushbutton when the STORE ENBL light is ON. Selection (SEL) of the rate that will control the frequency register when SWP is ON occurs when SEL ENBL is ON or as automatically advanced when the TRK and SWP lights are ON.

Figure 6 is a simplified logic diagram showing a typical stage of the rate register for manually storing four rates, addressing of one of the four rates to control the rate generator, and addressing of one of the four rates for front panel display. The display and control clock signals are derived from the 1-MHz clock that alternately enables selection of the rate number to be displayed or controls the rate generator, depending on the phase of the timing signal. When the timing signal is a logic 1 level, the number addressed with the read select code is transferred to the rate display buffer. The manual switch disables the front panel store, select and sweep control pushbuttons transferring control of the programmed oscillator to the computer as shown. The rate and limit selector pushbuttons permit operator monitoring under computer control.

Figure 7 is a simplified logic diagram of one of the decades of the stored start times. Four time numbers consisting of h:m:s are stored with the four corresponding stored rates. Depending on the sweep control logic status (TRK light ON and/or ACQ light ON), the stored time activates the related rate to produce a timed frequency ramp. A comparator senses equality between station time and the time related to the current selected rate to turn the SWP light ON if OFF. If the TRK light is ON and the ACQ light is OFF, the control logic selects the next stored time for equality comparison to produce a series of timed frequency ramps.

Station time is normally displayed except when a rate pushbutton is depressed to permit visual inspection of the corresponding stored time.

B. Synthesizer Modifications

The Model 7010-S-179 Dana Digiphase Synthesizer described in Ref. 1 was improved to provide increased phase control resolution and reduce radiated leakage of internally generated RF. The phase control resolution was extended to the 10^{-3} Hz control decade to reduce the incremental phase steps at X-band frequency (×168 multiplication) from 0.6-deg peak to less than 0.01-deg peak. This modification also improved the delay to output response of a 1-mHz frequency control increment from 10 s to approximately 40 μs. The packaging was modified to reduce radiated leakage; these modifications included the deletion of the unnecessary front panel controls, and the addition of RF gaskets and vent screens. The modified synthesizer is shown in Fig. 8.

IV. Programmed Oscillator Tracking Characteristics

The synthesizer output frequency tracks a programmed frequency ramp with a known constant delay and phase error. These errors and typical frequency ramp capabilities are described as follows:

A. Frequency Ramp Tracking Errors

The actual frequency ramp output of the digiphase synthesizer is delayed (offset) relative to the programmed ramp (Fig. 9). This offset is due to the inherent hardware computing rates that produce the digital frequency ramp and subsequently the related digital phase reference to the synthesizer phase-locked loop. The total delay in computing and converting the digital frequency ramp to an analog reference to the synthesizer loop is 40 μs $\pm$ 5 μs.

The synthesizer computes the phase reference from a programmed frequency control input during a period of two 10-μs sample intervals and then converts the digital result to an analog value in the next sample interval for a total delay of 30 μs. An additional sample period of 10 μs occurs in generating the frequency control ramp input to the synthesizer. An uncertainty of $\pm$5 μs is due to the random relationship of the station 1-s tick and the synthesizer phase computer sampling rate (100 kHz).

The effect of this delay in computing the digital ramp results in an accumulative phase error (Fig. 9), and results in an offset in doppler residuals. The following expressions represent the actual frequency ramp and phase output of the synthesizer except for small phase variations less than 1×10^{-7} cycle due to quantization effects that are not accumulative.

$$f_T = f_0 + \dot{f}(T - \tau) \qquad \text{(Hz)}$$

$$\phi_T = \omega_0 (T - \tau) + \frac{\dot{\omega}}{2} (T - \tau)^2 \qquad \text{(radians)}$$

where

$$\tau = 40\ \mu s \qquad \pm 5\ \mu s$$

The synthesizer phase-locked loop tracks the digital frequency ramp with a very small tracking error of less than 1.2×10^{-8} cycles/Hz/s.

The loop tracking error with a frequency ramp, A (Hz/s), applied to the loop reference phase input ϕ_R is given as follows:

For a frequency ramp, $\phi_R(t) = At^2$

$$L[\phi_R(t)] = \phi_R(S) = \frac{2A}{S^3}$$

The equation for the loop phase error ϕ_E with the ramp applied is:

$$\phi_\varepsilon(S) = \frac{1}{1 + G(S)} \phi_R(S)$$

where

$$G(S) = K\left(\frac{S\tau + 1}{S^2}\right) \text{ is the open loop gain.}$$

The loop error time response $\phi_\varepsilon(t)$ is then:

$$\phi_\varepsilon(t) = L^{-1}[\phi_\varepsilon(S)] = \frac{2A}{K}\left[1 - \frac{\varepsilon^{-\alpha t}}{\beta} \sin(\beta t + \psi)\right]$$

where

$$K = \alpha^2 + \beta^2 = 1.78 \times 10^8$$

$$\tau = 1.65 \times 10^{-4}\ \text{s}$$

$$\alpha = \frac{\tau K}{2}$$

$$\beta = \pm\sqrt{K - \alpha^2}$$

$$\psi = \tan^{-1}\frac{\beta}{\alpha}$$

The steady-state error term in the phase error time response to the frequency ramp ($2A/K$) is of interest:

$$\phi_\varepsilon(t)_{ss} = \frac{2A}{K} = \frac{2A}{(1.78 \times 10^8)}$$

This tracking error represents an offset of the output ramp relative to the reference ramp input of 1.1236×10^{-8} cycles/Hz/s and is a fixed offset in phase that does not accumulate with time.

B. Frequency Ramp Techniques

A variety of frequency ramping sequences can be derived, some of which are shown in Figs. 10a, 10b, 10c, and 10d.

Figure 10a illustrates a ramp sequence automatically initiated at T_0 and terminated at the stored upper limit (f_{UL}) as enabled with the TRK light ON and LIM ENBL light ON. Note that the sweep terminates at the limit towards which the sweep is advancing with LM ENBL light ON. Figure 10b illustrates a similar sequence with opposite polarities and use of the low limit (f_{LL}).

Figure 10c illustrates a triangular sweep between selected upper and lower frequency limits at a selected rate. This ramp sequence is initiated with the ACQ light ON with SWP start (SWP-ON) occurring at the selected rate time stored. Automatic reversal of the rate polarity occurs when the advancing frequency becomes greater than the limit reached. The figure illustrates a change entered to the upper limit and a resulting sweep termination at that limit when enabled as indicated by the LM ENBL light turned ON.

Figure 10d illustrates a ramp sequence of stored rates with R0, R1, and R2 refreshed with new rates as the sequence progresses. The termination, in this example, is at a selected upper limit (f_{UL}). The sequence is initiated by turning the TRK light ON. When the limit is reached, the sequence is terminated as indicated by the SWP and TRK lights OFF. Such a ramp sequence can be used for aided uplink or downlink doppler tracking.

Other combinations of ramp sequence can be generated to produce any desired frequency profile with ramp intervals as small as 1 s within a 24-h period.

Uplink (exciter) frequency ramping was used at DSS 14 and DSS 43 during the Pioneer 10 Jupiter flyby. Uplink frequency ramping was used to return the spacecraft receiver to best-lock frequency prior to entering Io occul-

tation and subsequently at the Jupiter occultation to facilitate recapture of two-way lock after exit. Additional ramping was used to insure recapture of two-way lock after exit from Io occultation and to provide coherent doppler tracking up to 30 min before periapsis.

A tuned oscillator range analysis (TORA) experiment was performed at DSS 14 using the programmed oscillators as reported in Ref. 3. Frequency ramping of the uplink to Pioneer 10 was completed with received two-way doppler data compared to a locally generated reference.

V. Conclusion

Block III receiver/exciters at DSSs 14 and 43, utilizing the programmed oscillators, were used to track Pioneer 10 Jupiter encounter. The results are described below.

A. Doppler Phase Jitter

Doppler jitter measurements [using (Ref. 4)] taken at DSS 14 by the Network Systems Support Group both before and after the programmed oscillators were installed are tabulated in Table 1. Measurements at DSS 43 were not completed at the time of this article.

B. Doppler Residuals While Ramping

Analysis of ramped radio metric data as processed by the pseudo-residual program indicated that the doppler data noise while ramping was similar to the noise encountered with a constant frequency.

Pioneer 10 commands were sent to the spacecraft during frequency ramps without any associated errors occurring.

References

1. Wick, M. R., "DSN Programmed Oscillator Development," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VIII, pp. 111–124. Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1972.
2. Donnelly, H., and Wick, M. R., "Programmed Oscillator Development," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. X, pp. 180–185. Jet Propulsion Laboratory, Pasadena, Calif., Aug. 15, 1972.
3. Liu, A., "Range Measurements to Pioneer 10 Using the Digitally Controlled Oscillator," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. X, pp. 180–181. Jet Propulsion Laboratory, Pasadena, Calif., Aug. 15, 1972.
4. *Doppler System Evaluation Test*, DSIF Standard Test Procedure 853-60/2B-11. Jet Propulsion Laboratory, Pasadena, Calif., Sept. 15, 1973. (JPL internal document.)

Table 1. Doppler (degrees rms phase jitter)

Signal source	Before		After	
	Theoretical	Actual	Theoretical	Actual
Test transmitter:				
Signal level: 120 dBm	7.2	5.9	7.2	5.6
Signal level: 162 dBm	20.1	22.6[a]	20.1	23.0[a]
Test translator:				
Signal level: 120 dBm	2.8	2.3	2.8	2.5
Signal level: 160 dBm	20.9	—[b]	20.9	23.0[a]

[a]Values high due to signal level setting using old AGC curves.
[b]Not available.

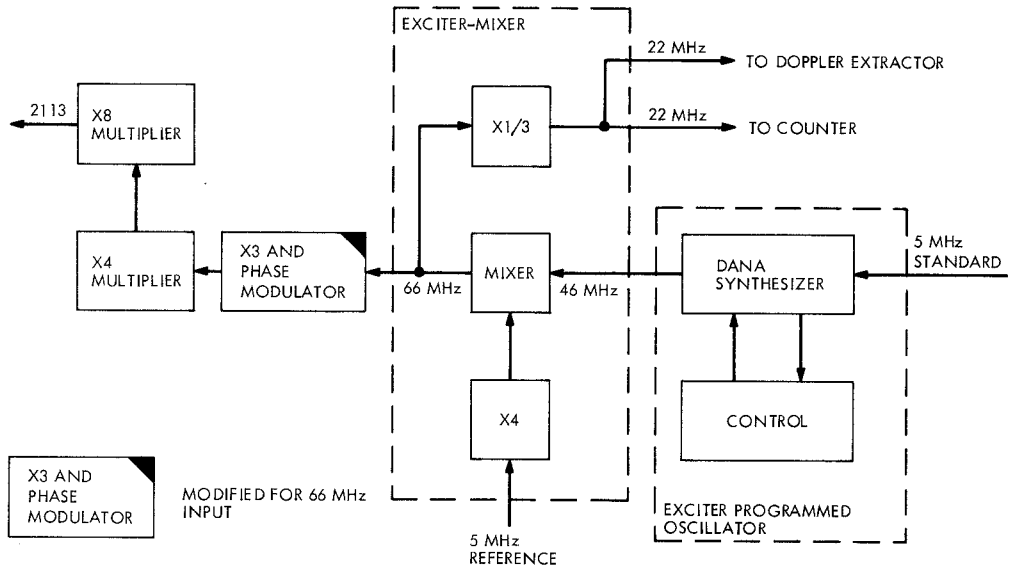

Fig. 1. Exciter modification block diagram

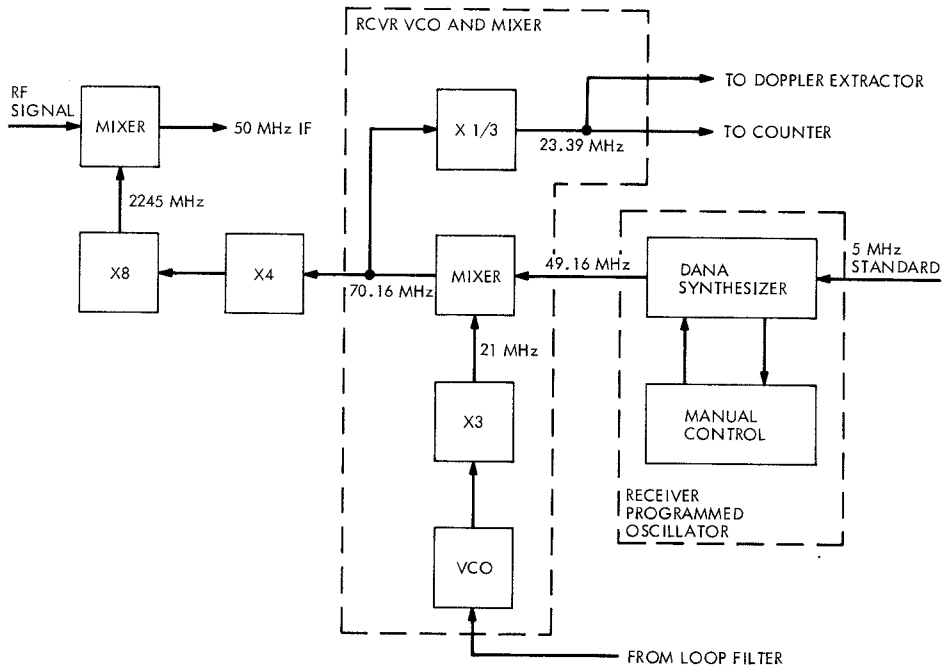

Fig. 2. Receiver modification block diagram

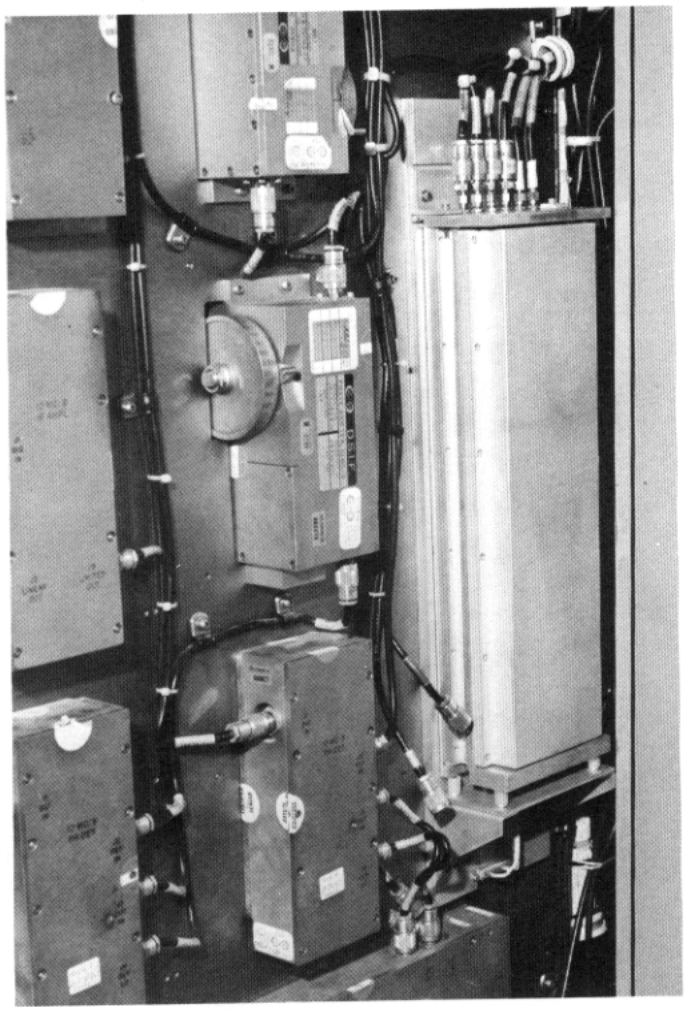

Fig. 3. RF subassembly installation

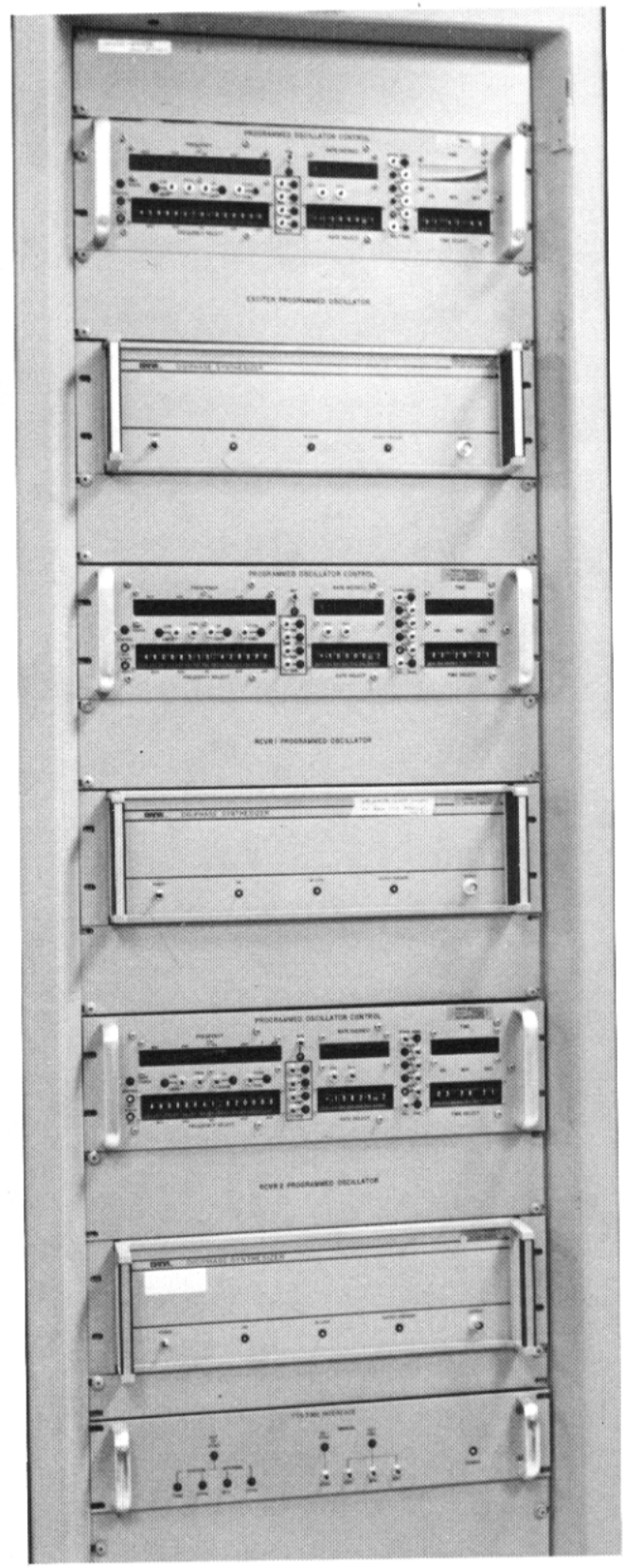

Fig. 4. Programmed oscillator cabinet assembly

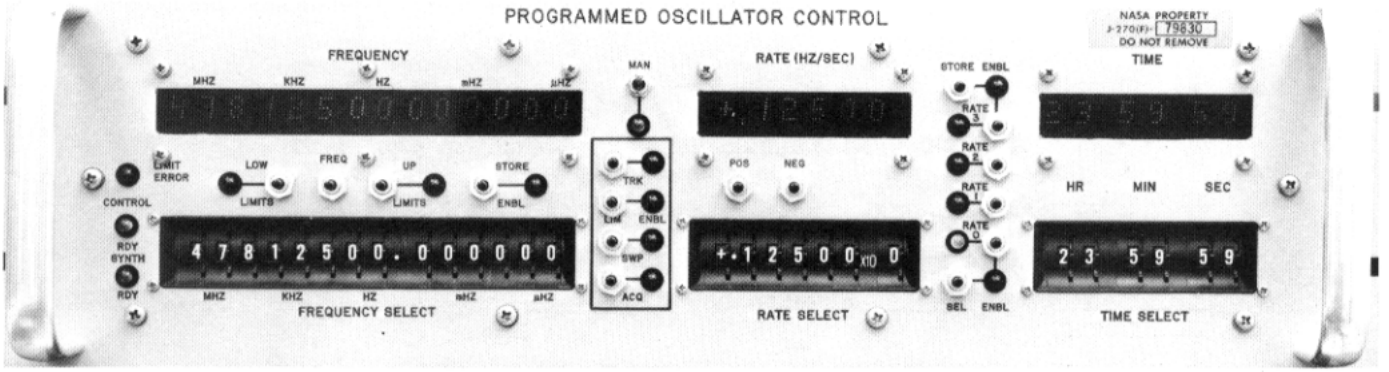

Fig. 5. Front panel control

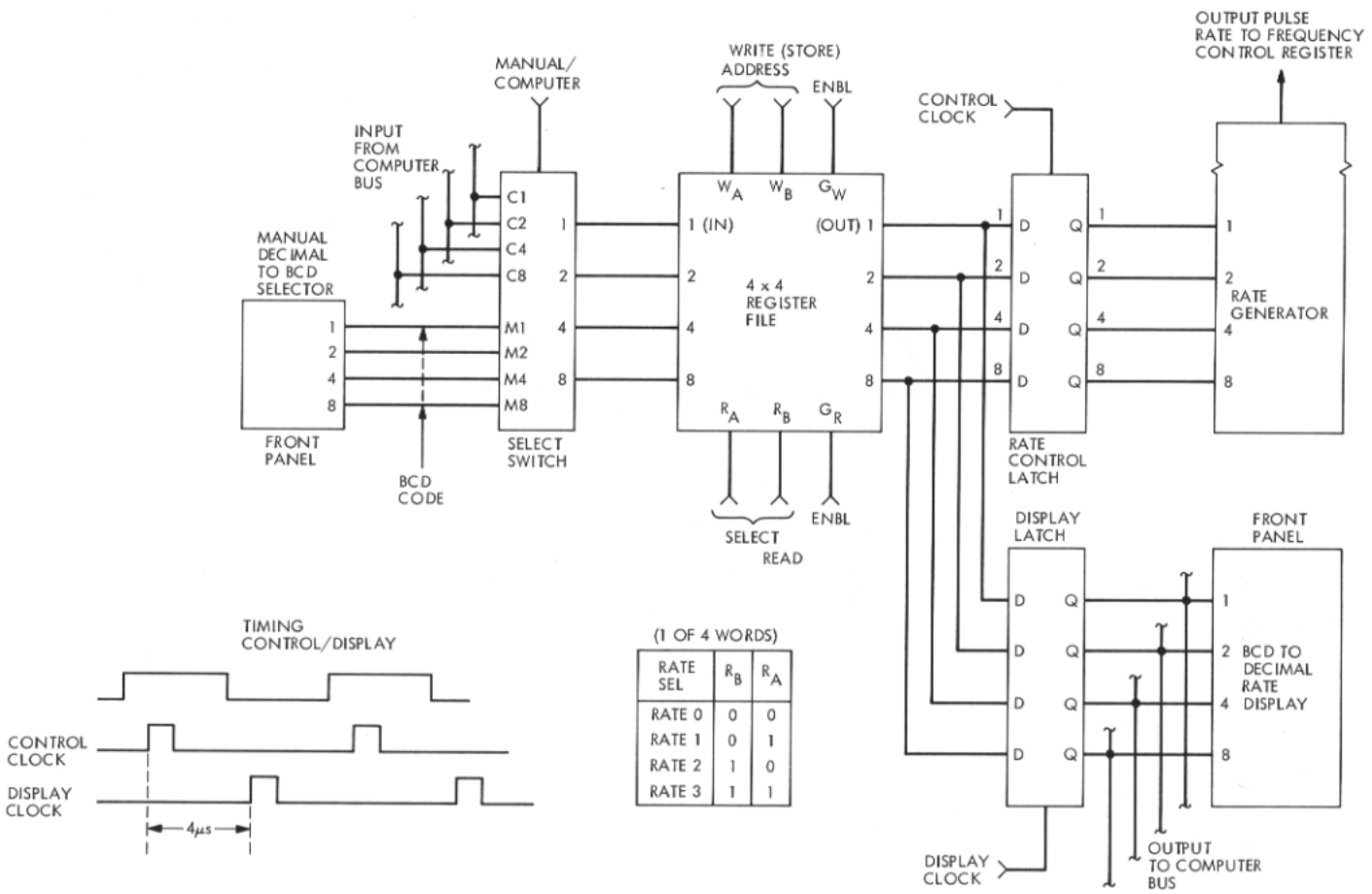

Fig. 6. Rate decade control and display logic

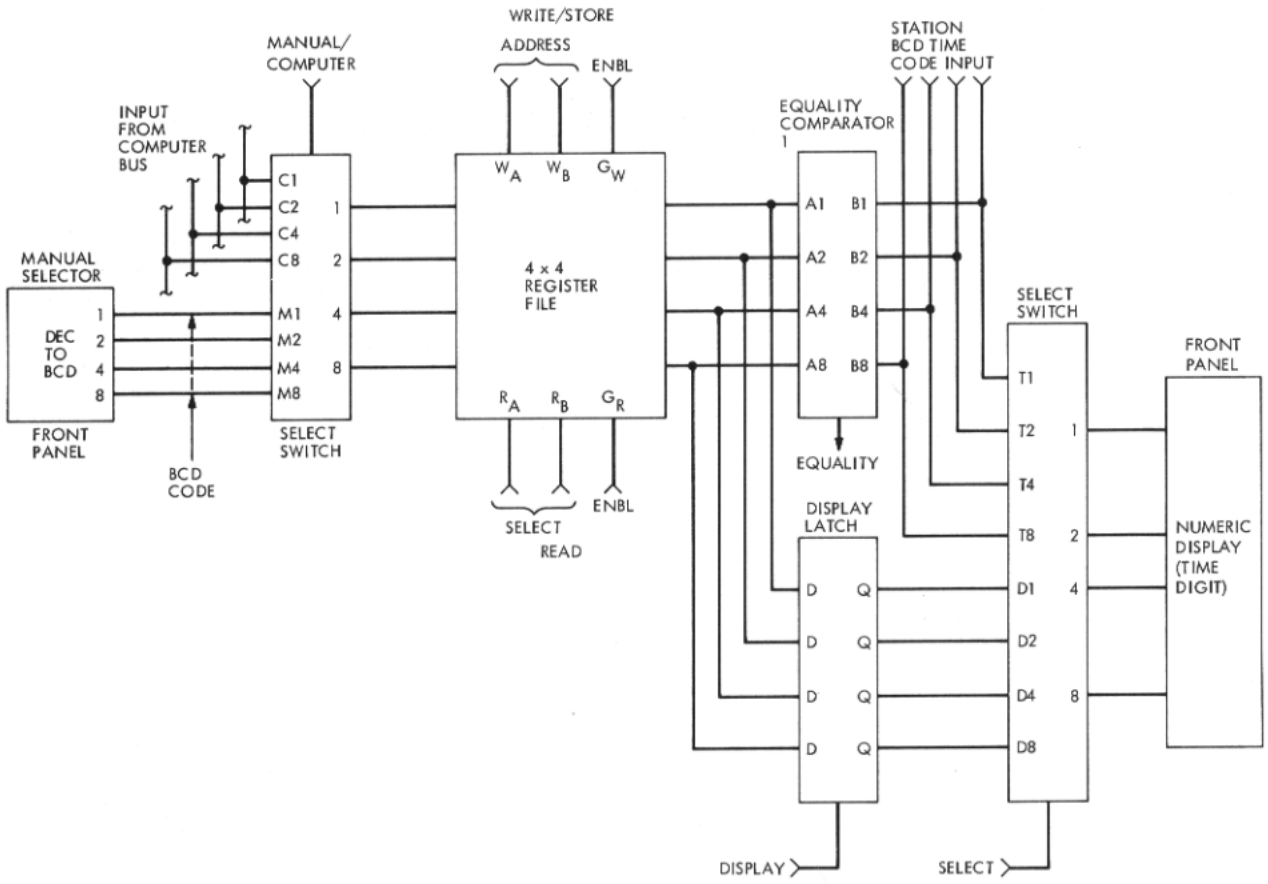

Fig. 7. Time decade control and display logic

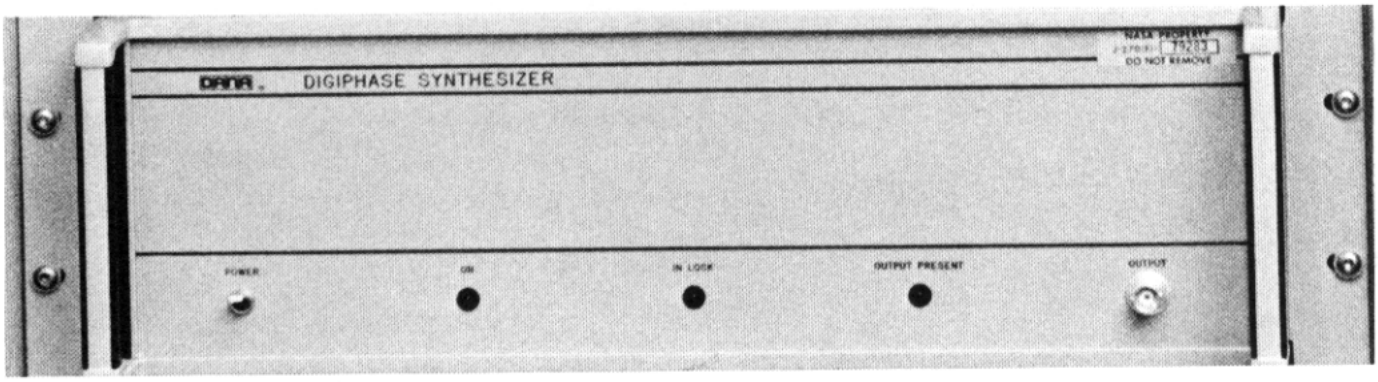

Fig. 8. Synthesizer

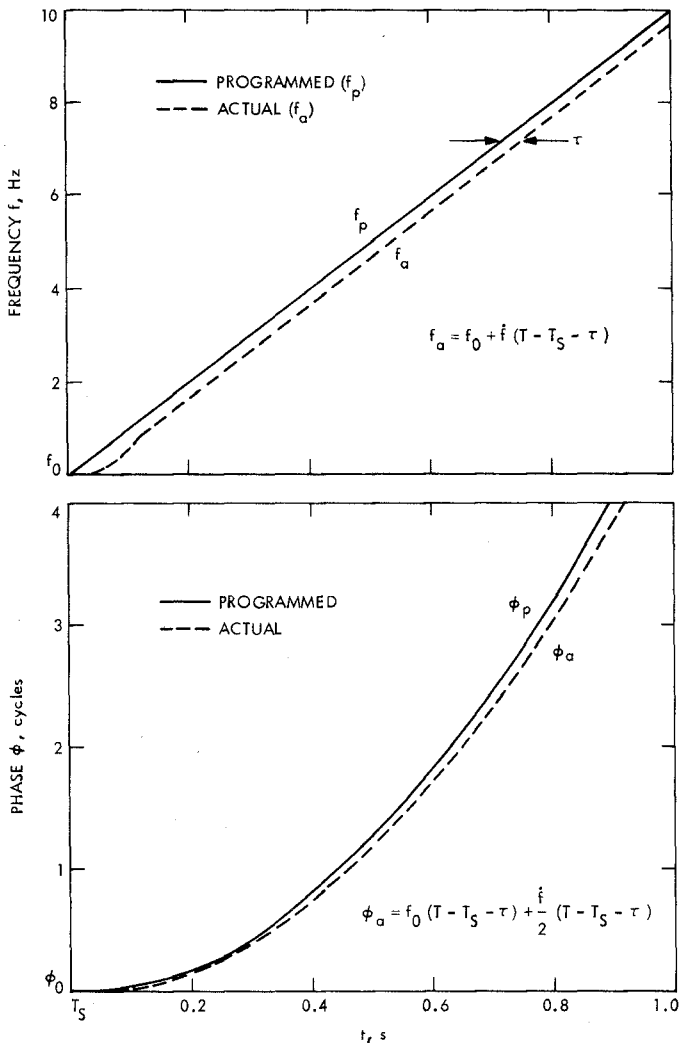

Fig. 9. Ramp errors

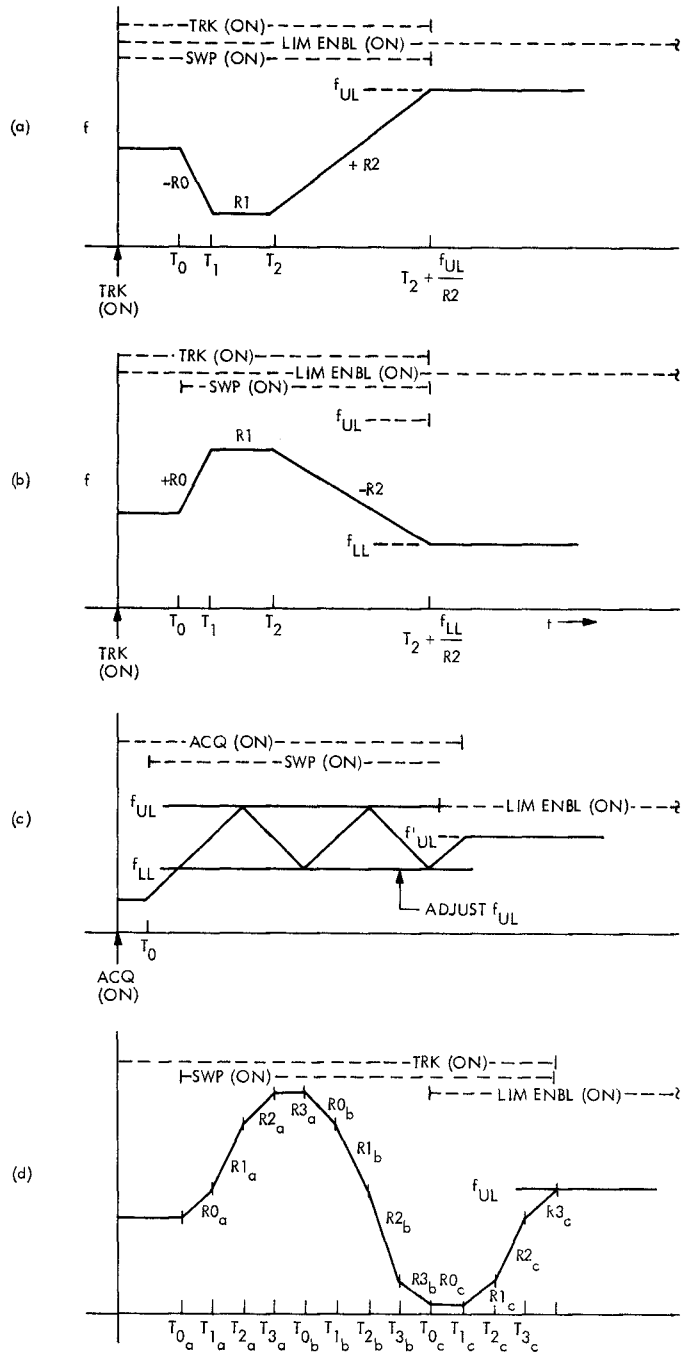

Fig. 10. Programmed ramp sequences; (a) triangular, automatically initiated at T_0, (b) opposite polarities and the low limit, (c) selected upper and lower frequency limits, (d) typical tracking sequence.